REMARKS

Claims 1 and 4-8 have been amended. Claims 1-11 remain pending in this application.

Claims 1-4 and 6 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,861,771 to Matsuda et al. ("Matsuda"). The rejection is respectfully traversed.

Claim 1 has been amended to recite "an output driver... wherein the output driver is a MOS transistor", "a diode inserted between the gate and the source of the MOS transistor, the diode having a reverse breakdown voltage lower than an oxide breakdown voltage of the MOS transistor," and "a constant current inverter inserted between a power supply line and the output driver." Matsuda does not disclose these limitations.

In rejecting claim 4, the Office Action refers to the current circuit mirror 62 of Matsuda as teaching a diode. In rejecting claim 6, the Office Action refers to the current circuit mirror 62 as teaching a constant current circuit. As amended, claim 1 of the present application recites a semiconductor device incorporating both a diode and a constant current inverter. Matsuda does teach, suggest or disclose incorporating both of these elements. Claim 1 is therefore allowable over Matsuda.

Claims 2-4 and 6 depend from claim 1 and are allowable over Matsuda along with claim 1, as well as on their own merits. Accordingly, Applicant respectfully requests the rejection be withdrawn and the claims allowed.

Claims 5 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Matsuda. The rejection is respectfully traversed.

Claims 5 and 7 depend from claim 1 and are allowable over Matsuda along with claim 1, as well as on their own merits. Accordingly, Applicant respectfully requests the rejection be withdrawn and the claims allowed.

Claims 8 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Matsuda in view of U.S. Patent No. 5,936,460 to Iravani. The rejection is respectfully traversed.

Claim 8 has been amended to recite "a diode inserted between a gate and a source of the MOS transistor." Similar to claim 1, claim 8 recites both a diode and a "constant current circuit." Matsuda does not disclose these limitations, as explained above. Claim 8 is therefore allowable over Matsuda.

Iravani is cited for teaching a constant current circuit inserted between a power supply line and a combination of a reference voltage generating circuit and a differential amplifier circuit. The Office asserts that it would have been obvious to combine the current circuit taught by Iravani with the regulator circuit taught by Matsuda "to provide a stable, noise-free output current."

Iravani teaches a "current source having a high power supply rejection ratio," a circuit designed provide a noise-free current to noise sensitive circuits. Under the Office Action's proposal, the Iravani circuit is included within the Matsuda circuit to feed a stable, noise-free current to the output transistor 63. There are several problems with this.

First, Matsuda teaches a regulator circuit for stepping down a power supply, which is not a noise sensitive circuit for which Iravani is designed for use in. Iravani provides example circuits for which it is intended: "frequency synthesizers, signal generation (e.g., serial clock recovery), most circuits incorporating voltage controlled oscillators (VCO), and the like ... circuits which are ... particularly sensitive to electronic noise." Iravani described these as "circuits [that] cannot function properly in the presence of even small amounts of power supply noise." Iravani Col. 1, lines 17-22. On a broad level, noise is not an issue in a Matsuda regulator circuit to the point where it "cannot function properly in the presence of even small amounts of power supply noise", but even more specifically, it is certainly not an issue at output transistor 63 to a level where including an entire other circuit to provide noise-free current would make sense. The Office Action proposes that it would be obvious to include an Iravani current source circuit with the output transistor 63 as the receiving circuit. Applicant respectfully submits that such a move would be highly impractical,

and the costs far outweigh the benefit, of which there is practically none sense the output transistor 63 has no such noise-sensitive need.

Second, Matsuda specifically teaches against such an inclusion. As Matsuda describes in its Background of the Invention, one of the primary problems with the known art is occupation of too much area on a chip. An objective of Matsuda is to provide a regulator circuit which "occupies a reduced area on a chip." Matsuda col. 2, lines 20-21. Since noise is not an issue in Matsuda, but chip area is an important issue, it would go against the teaching of Matsuda to increase the amount of chip area to combat noise. In essence, it would provide an unneeded additional feature that wastes valuable chip area. Accordingly, Applicant submits that Iravani should not be combined with Matsuda as the basis for a §103 rejection.

As Matsuda does not teach all of the limitations of claim 8, and since a Matsuda regulator circuit is not a highly noise-sensitive circuit that would benefit from inclusion of an Iravani current source circuit, and further teaches against increasing chip area, claim 8 is allowable over Matsuda and Iravani. Claim 11 depends from claim 8 and is allowable over Matsuda and Iravani along with claim 8 as well as on its own merits. Accordingly, Applicant respectfully requests the rejection be withdrawn and the claim allowed.

Claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Matsuda and Iravani in view of U.S. Patent Publication No. 2004/0046532 to Menegoli et al. ("Menegoli"). The rejection is respectfully traversed.

Claims 9 and 10 depend from claim 8 and are allowable over Matsuda and Iravani along with claim 8 for at least the reasons provided above as well as on their own merits. Menegoli is cited for teaching that MOSFET transistors can be made either in enhancement or depletion by adjusting the surface concentration of the channel region and fails to cure the deficiencies of Matsuda and Iravani identified above. Claims 9 and 10 are therefore allowable over the combination of Matsuda, Iravani and Menegoli. Accordingly, Applicant respectfully requests the rejection be withdrawn and the claim allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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